

FIGURE I

Adjustable Start Times

Fixed End Times

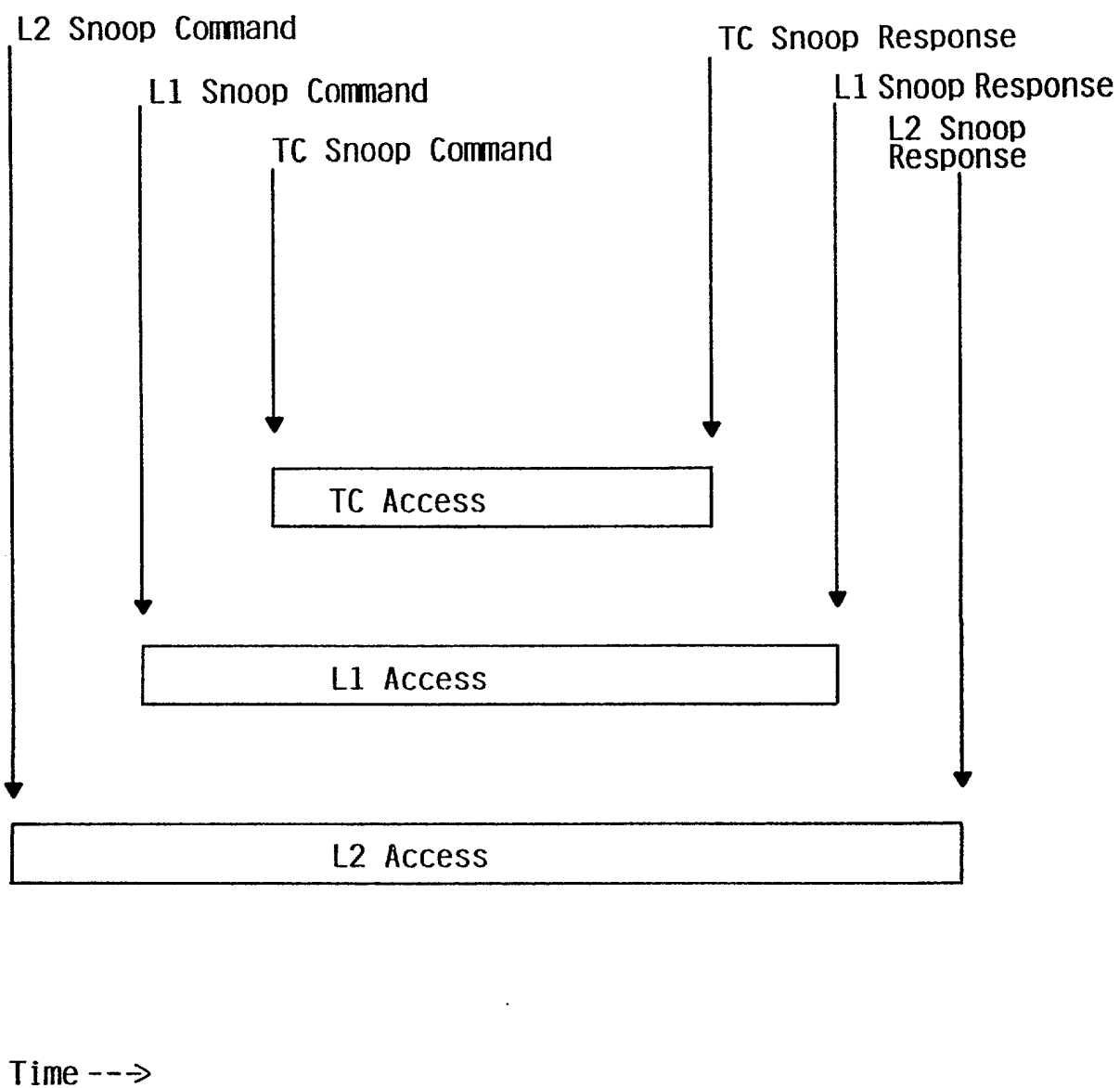


FIGURE 2

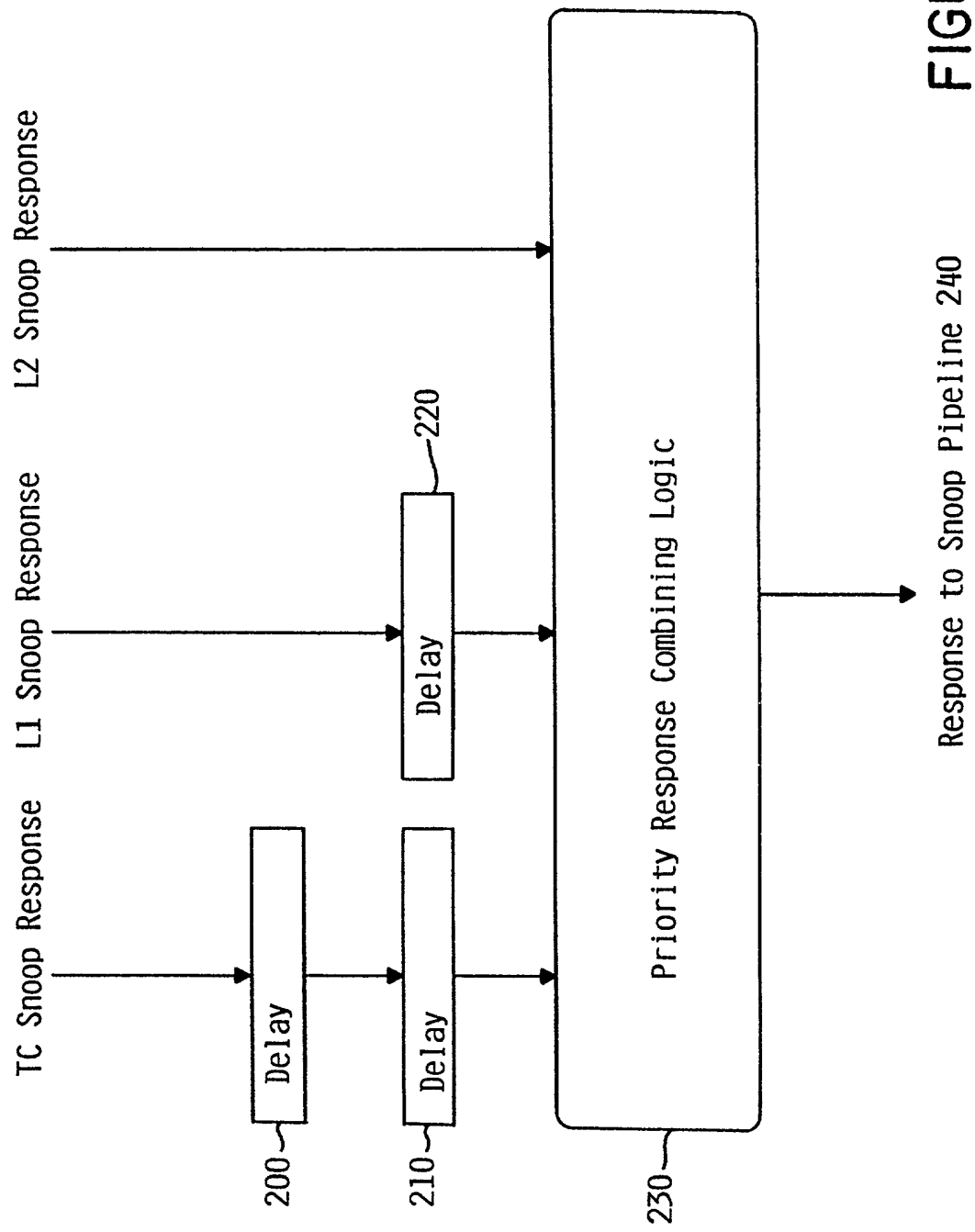


FIGURE 3

TC Response	L1 Response	L2 Response	Combined Response
Retry	Any	Any	Retry
Any	Retry	Any	Retry
Any	Any	Retry	Retry
Modified	Not Retry	Not Retry	Modified
Not Retry	Modified	Not Retry	Modified
Not Retry	Not Retry	Modified	Modified
Shared	Shared/Null	Shared/Null	Shared
Shared/Null	Shared	Shared/Null	Shared
Shared/Null	Shared/Null	Shared	Shared
Null	Null	Null	Null

FIGURE 4

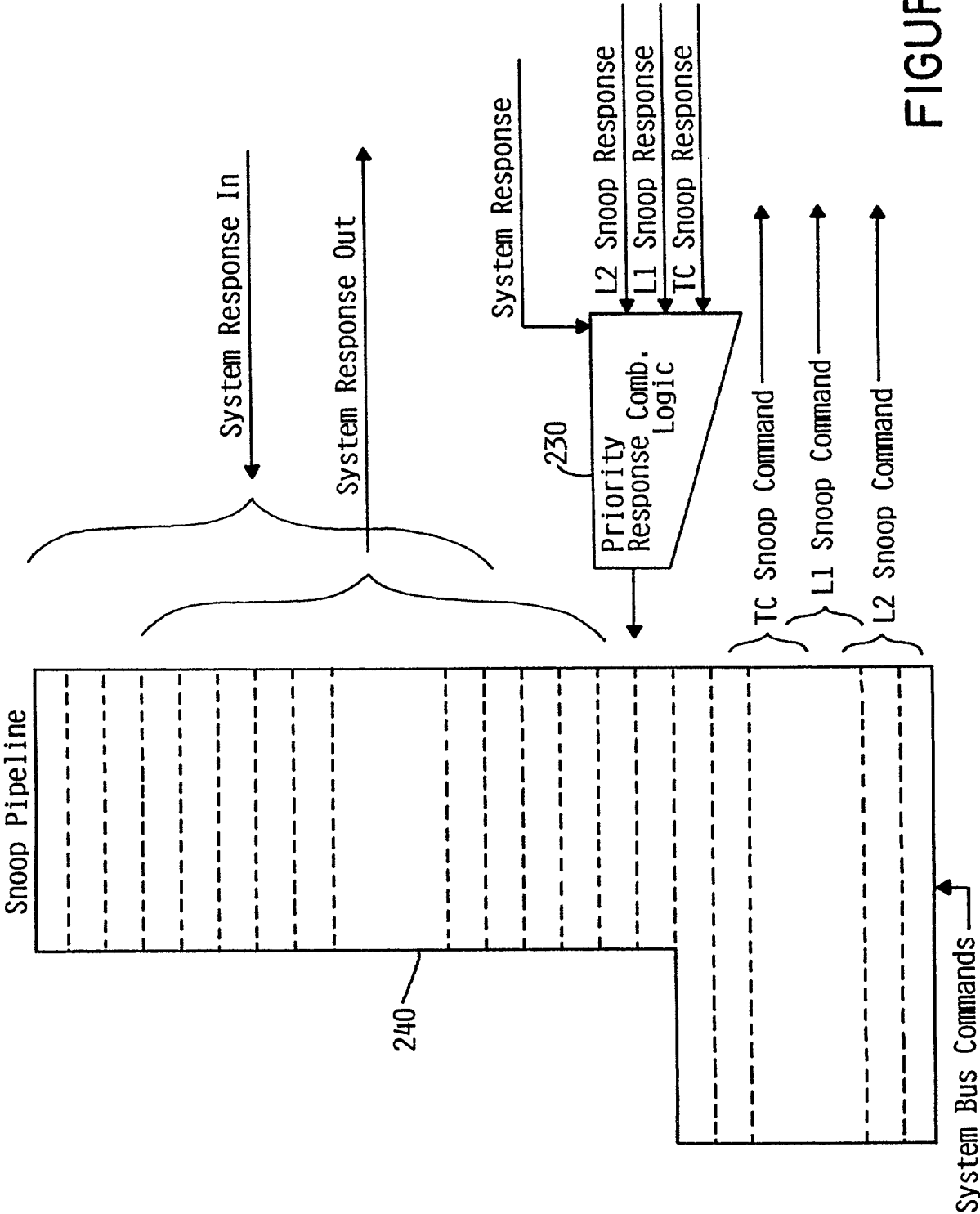


FIGURE 5

Pipelined Overlapping Snoops 6/12

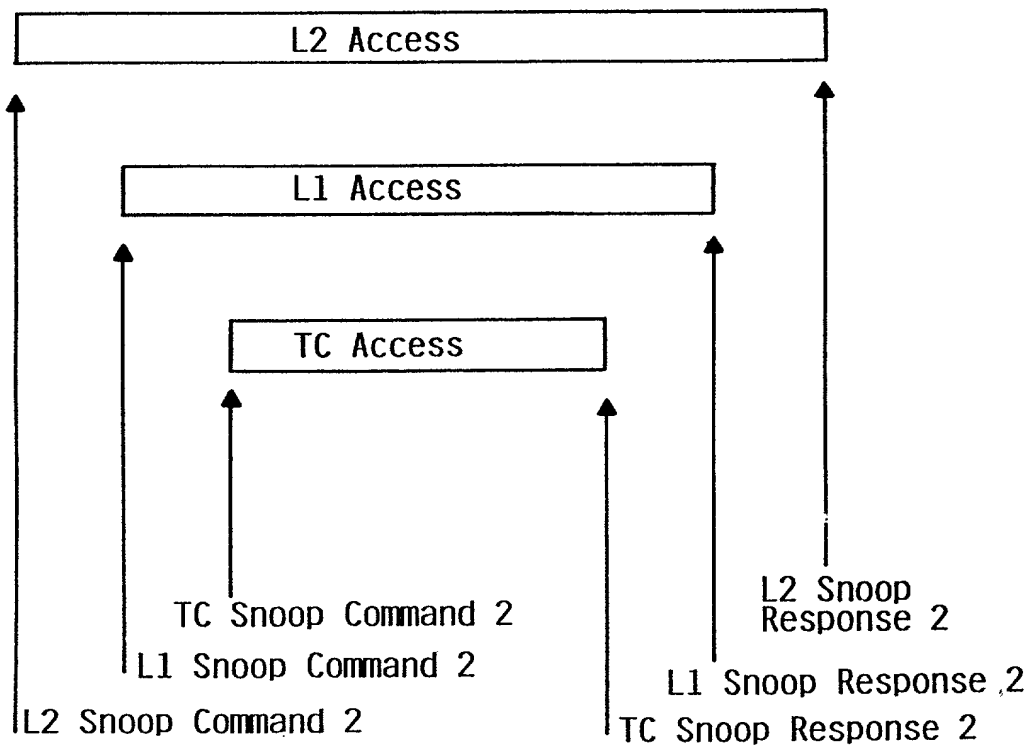
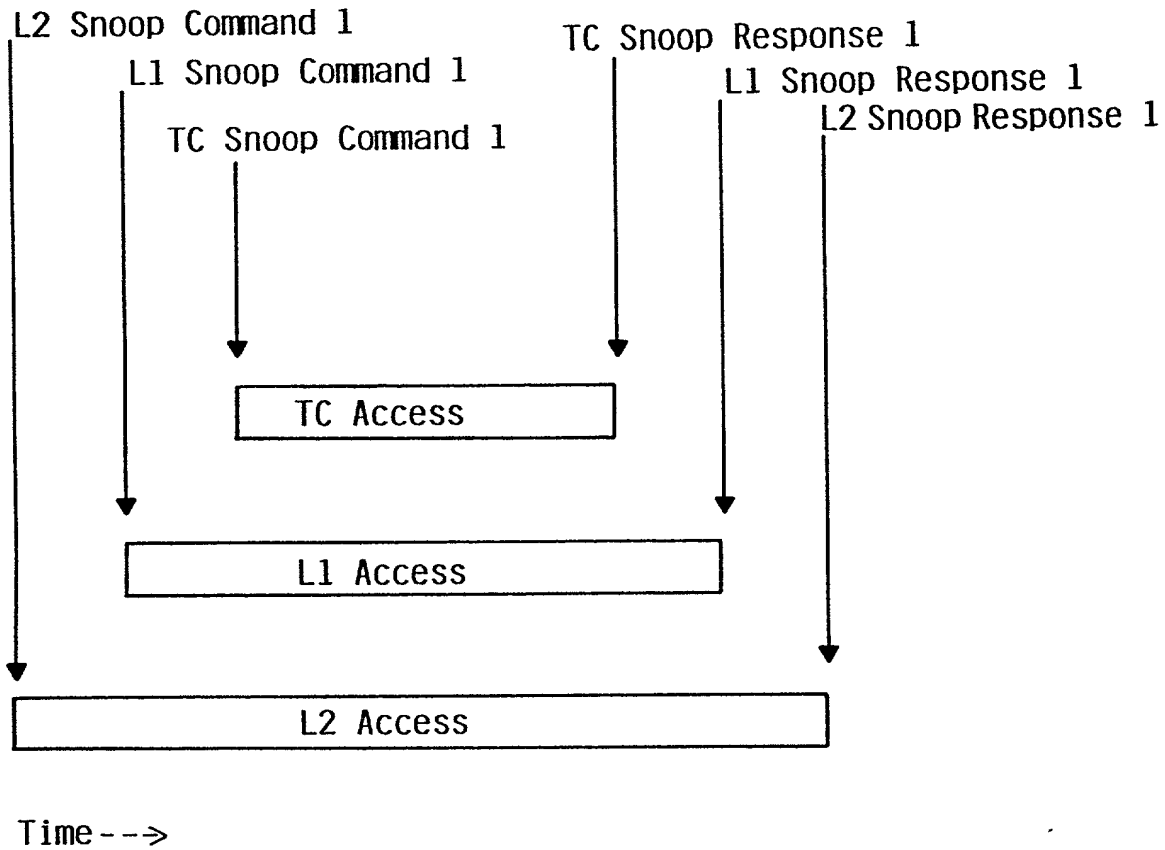


FIGURE 6

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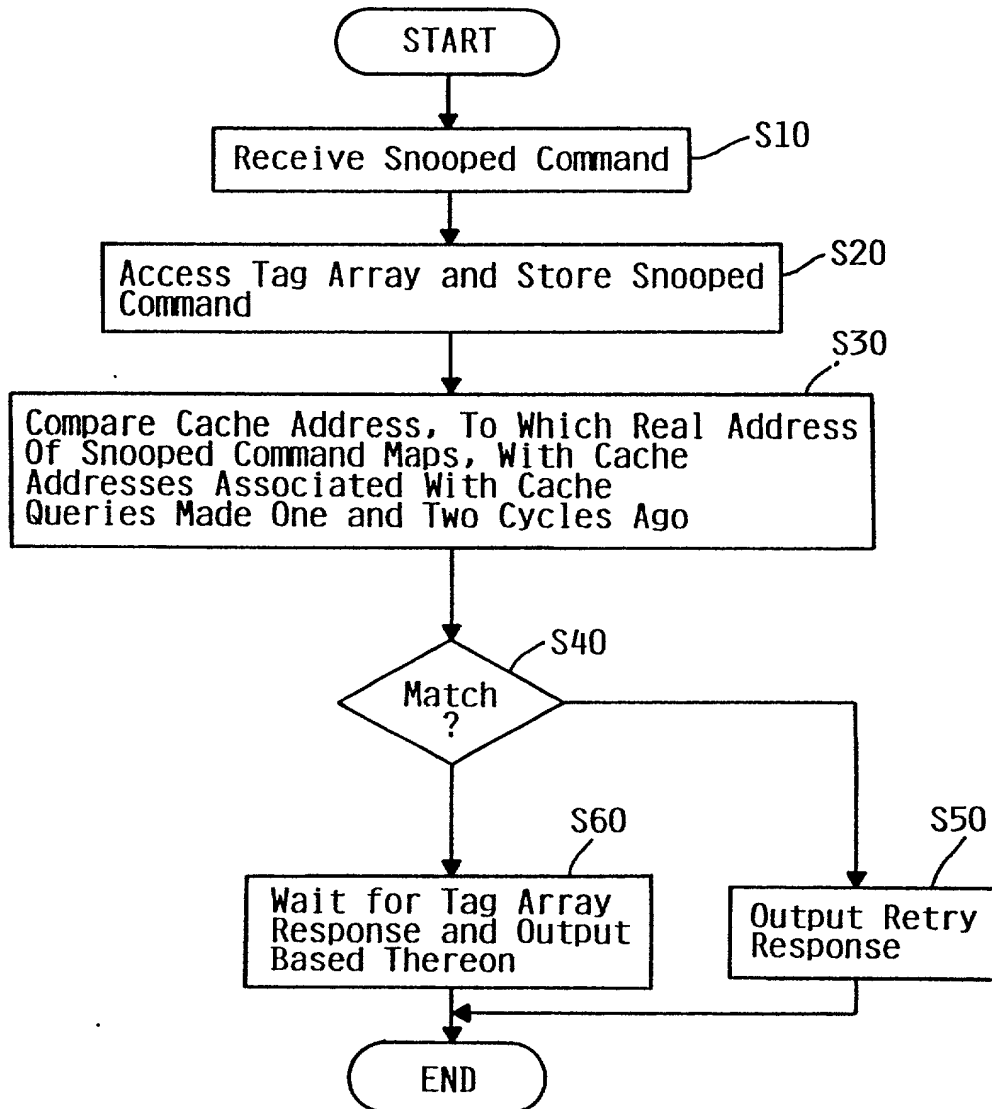


FIGURE 7

L(n) Response	L(n+1) MESI	L(n+1) Response
Retry	No Change	Any
Modified	No Change	Retry
Modified	MESI->I	Not Retry
Shared	No Change	Retry
Shared	M	
Shared	ES->SI	Shared
Shared	I	Null
Null	No Change	Retry
Null	M->MSI	Modified
Null	ES->SI	Shared
Null	I	Null

FIGURE 8

Snooped Second Command from System Bus	L1/L2 Cache State	TC Response	System Response to First Command	Combined Response
Exclusive	Unknown	Retry	Not Applicable	Retry
Exclusive	Known and Invalid	Retry	Not Applicable	Retry
Non-Exclusive	Unknown	Retry	Not Applicable	Retry
Non-Exclusive	Known and Invalid	Conditional Retry	Retry	Not Retry
Non-Exclusive	Known and Invalid	Conditional Retry	Not Retry	Retry

FIGURE 9

L1 State	L2 State	System Coherency Response Received	System Bus Command Out
Modified->Invalid	MESI->I	Not Retry	None
Modified->Invalid	MESI->I	Retry	Write to memory
ESI->I	Modified->Invalid	Not Retry	None
ESI->I	Modified->Invalid	Retry	Write to memory

FIGURE 10

This Processor's Command	Snooped Command from System Bus	This processor's TCache State	Has Data Started to Arrive for this Access?	This Processor's TCache Response	This Processor's new TCache State
Non-Exclusive	Exclusive	E,S,0	No	Null	I
Non-Exclusive	Exclusive	E,S,0	Yes	Retry	Unchanged
Non-Exclusive	Non-Exclusive	E,S,0	No	Shared	S
Non-Exclusive	Non-Exclusive	E,S,0	Yes	Retry	Unchanged
Exclusive	Not Applicable	M	Not Applicable	Retry	Unchanged
Exclusive	Not Applicable	E	Not Applicable	Retry	Unchanged

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FIGURE 11

L1 State	L2 State	System Coherency Response Received	System Bus Command Out
Modified->S,I	MESI->I	Not Retry	None, Source data
Modified->S,I	MESI->I	Retry	Write to memory
ESI->I	Modified->S,I	Not Retry	None, Source data
ESI->I	Modified->S,I	Retry	Write to memory
ESI->S,I	EOS->S,I	Not Retry	None, Source data
ESI->S,I	EOS->S,I	Retry	None, Discard data

FIGURE 12